ABSTRACT OF THE DISCLOSURE

A circuit using modular based parallel processing calculates the cumulative parity of a binary number input sequence. The circuit is used, for example, to implement a precoder for an optical duobinary transmission system. The design permits a relatively low-speed circuit to be used as the precoder before a time-division multiplexer. The parallel circuit can be scalable to process a very large number of sets of parallel binary data by the usage of two basic modules, namely, a parity module and a delay module.